REMARKS

In response to the final Office Action dated 4 January 2001, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 21, 23, 24, 26, 29-33 and 36-75 are pending in the application, and are rejected. Claims 43, 46, 47, 50, 53-55, 58-60, 62, 65, 67, 68, 70, 73, and 75 have been amended. No new matter has been added.

Rejection Under 35 USC § 112

Claims 60-75 were rejected under 35 USC § 112, second paragraph. The applicant respectfully traverses. Claims 68, 70, 73, and 75 have been amended to obviate the rejection.

Rejections Under 35 USC § 103

Claims 21, 23, 24, 26, 29-33 and 36-75 were rejected under 35 USC § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,449,941, Yamazaki) in view of Halvis et al. (U.S. Patent No. 5,369,040, Halvis). The applicant respectfully traverses.

Claim 21 recites a method of fabricating a transistor in a semiconductor substrate including, among other elements, forming a source region and a drain region, a channel region being between the source region and the drain region, forming an insulating layer on the channel region, forming a gate on the insulating layer, wherein the gate comprises a silicon carbide compound $Si_{1-x}C_x$, and selecting x to be between 0 and 1.0.

Yamazaki is deficient as a reference in the following respects. Yamazaki discloses in Figures 2A-2D steps for forming a memory cell with a source region 203, a drain region 204, an oxide film 205, a floating gate 208, and a control gate 210. However, as the Examiner stated, Yamazaki does not disclose forming a gate on an insulating layer, wherein the gate comprises a silicon carbide compound $Si_{1-x}C_x$, as recited in claim 21.

Halvis discloses a MOS photodetector with closely-spaced gates 34, 36, 38, 48, and 50 shown in Figure 4C. The gates comprise polysilicon and carbon. However, Halvis does not disclose forming a source region and a drain region, a channel region being between the source region and the drain region, and forming an insulating layer on the channel region as recited in claim 21.

The Examiner stated that it would have been obvious to one of ordinary skill in the art to replace the gate of Yamazaki with the gate disclosed by Halvis. The applicant respectfully traverses. There must be a showing of a "teaching or motivation to combine prior art references" to support a rejection under section 103 and "the showing must be clear and particular." *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Such a showing of a "teaching or motivation to combine" is necessary to avoid the use of hindsight when combining references under section 103. 50 USPQ2d at 1616-17.

There is no teaching in either Yamazaki or Halvis for the combination put forward by the Examiner. Yamazaki discloses a memory cell with a source region 203, a drain region 204, a floating gate 208, and a control gate 210. Halvis discloses a MOS photodetector with multiple gates and no source or drain. The structures are very different and operate in a different manner, so one skilled in the art would not find a teaching in either for the combination. For example, the memory cell of Yamazaki is used to store charge on the floating gate 208. In contrast, the gates of Halvis have improved transparency to visible light to improve the quantum efficiency of a photodetector that detects photons passing through the gates. Also, Halvis discloses multiple gates that are spaced closely together, and there is no teaching that only one of the Halvis gates comprising polysilicon and carbon would be advantageous in the transistor of Yamazaki. Neither Yamazaki nor Halvis teach that Yamazaki would be improved by the addition of only one of the gates of Halvis.

Furthermore, Yamazaki teaches away from the combination. The invention of Yamazaki includes a thin insulator 105 of silicon carbide formed selectively on a part of the drain 104 shown in Figures 1B to 1D. Column 4, lines 7-14 and 27-29 and column 6, lines 1-9. The

silicon carbide insulator 105 is directly between the drain 104 and the floating gate 107. Therefore, one skilled in the art would not have been motivated to form either the floating gate 107 or the control gate 109 shown in Figure 1D from the same material as the insulator 105.

The Examiner stated on pages 3 and 6 of the final office action that it would have been obvious to replace the polysilicon gate of Yamazaki with the gate taught by Halvis "because of the desirability to improve response, to improve quantum efficiency, and to improve performance and light sensitivity." These reasons are from the Examiner, not from either Yamazaki or Halvis as is required by *In re Dembiczak.* The Examiner is improperly using hindsight to combine Yamazaki and Halvis.

The applicant respectfully submits that claim 21 is not disclosed or suggested by the combination of Yamazaki and Halvis, and that claim 21 is in condition for allowance. Claims 23, 24, 26, 29-33 and 36-42 are dependent on claim 21, and recite further limitations with respect to claim 21. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 23, 24, 26, 29-33 and 36-42 are not disclosed or suggested by the combination of Yamazaki and Halvis, and that claims 23, 24, 26, 29-33 and 36-42 are in condition for allowance.

Claims 43-75 recite limitations similar to those recited in claim 21. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 43-75 are not disclosed or suggested by the combination of Yamazaki and Halvis, and that claims 43-75 are in condition for allowance.

Claims 43-45, 48-51, 55-57, 60, 61, 65, 66, 68, 69, and 71-74 were rejected under 35 USC § 103(a) as being unpatentable over Halvis in view of Tohyama (U.S. Patent No. 5,858,811). The applicant respectfully traverses.

Claim 43 recites a method of fabricating a transistor comprising, among other elements, forming a source region and a drain region in a substrate that are separated by a channel region in the substrate.

Halvis is deficient as a reference in that Halvis does not disclose forming a source region and a drain region in a substrate that are separated by a channel region in the substrate as recited in claim 43.

Tohyama does not supply the elements missing in Halvis. Tohyama discloses a charge coupled device that does not have a source region or a drain region as recited in claim 43. Therefore, even as combined, Tohyama and Halvis do not disclose or suggest all of the elements recited in claim 43.

In addition, the Examiner has not pointed to specific language in either Halvis or Tohyama that is a teaching to combine them as is required by *In re Dembiczak.*

The applicant respectfully submits that claim 43 is not disclosed or suggested by the combination of Tohyama and Halvis, and that claim 43 is in condition for allowance. Claims 44, 45, 48, and 49 are dependent on claim 43, and recite further limitations with respect to claim 43. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 44, 45, 48, and 49 are not disclosed or suggested by the combination of Tohyama and Halvis, and that claims 44, 45, 48, and 49 are in condition for allowance.

Claims 50, 51, 55-57, 60, 61, 65, 66, 68, 69, and 71-74 recite limitations similar to those recited in claim 43. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 50, 51, 55-57, 60, 61, 65, 66, 68, 69, and 71-74 are not disclosed or suggested by the combination of Tohyama and Halvis, and that claims 50, 51, 55-57, 60, 61, 65, 66, 68, 69, and 71-74 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

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Signature

Docket No. 303.324US2 Micron Ref. No. 96-1051.01
WD #306382

Clean Version of Pending Claims

TRANSISTOR WITH VARIABLE ELECTRON AFFINITY GATE AND METHODS OF FABRICATION AND USE
Applicant: Leonard Forbes et al.
Serial No.: 09/256,643

Claims 21, 23, 24, 26, 29-33 and 36-75, as of May 4, 2001 (RCE filed).

21. A method of fabricating a transistor in a semiconductor substrate, the method comprising:

forming a source region and a drain region in a semiconductor substrate, a channel region being between the source region and the drain region;

forming an insulating layer on the channel region;

forming a gate on the insulating layer, wherein the gate comprises a silicon carbide compound $Si_{1-x}C_x$; and

selecting x to be between 0 and 1.0.

23. The method of claim 21, wherein x is selected such that a barrier energy between the gate and the insulator is between 0 eV and 2.8 eV.

24. The method of claim 21, wherein x is selected at a predetermined value that is between 0.5 and 1.0.

26. The method of claim 21 wherein x is selected such that the transistor has a charge retention time of between 1 second and 10^6 years.

29. The method of claim 21, wherein forming a gate further comprises:

depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer using low pressure chemical vapor deposition to form a layer of gate material; and

etching the gate material to a desired pattern using a reactive ion etch process.

30. The method of claim 29 wherein etching the gate material further comprises using plasma etching in combination with the reactive ion etch process.

31. The method of claim 29, further comprising conductively doping the silicon carbide compound $Si_{1-x}C_x$ while depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer.

32. The method of claim 29, further comprising oxidizing the gate to form a thin layer of oxide on the gate.

33. The method of claim 21wherein the gatecomprises a floating gate, and further comprising:

forming an intergate dielectric over the floating gate; and

forming a polysilicon control gate over the intergate dielectric.

36. The method of claim 21 wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on the channel region by dry thermal oxidation.

37. The method of claim 21 wherein forming a source region comprises forming a p-type source region and a p-type drain region in an n-type silicon substrate, a channel region being between the p-type source region and the p-type drain region.

38. The method of claim 21 wherein forming a source region comprises forming an n-type source region and an n-type drain region in a p-type silicon substrate, a channel region being between the n-type source region and the n-type drain region.

39. The method of claim 21 wherein forming a gate further comprises doping the gate by ion implantation.

40. The method of claim 21 wherein forming a gate further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

41. The method of claim 40 wherein depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer further comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer.

42. The method of claim 21, further comprising:

forming a well region in the semiconductor substrate;

forming field oxide on the semiconductor substrate to define an active region;

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

43. (Twice Amended) A method of fabricating a transistor comprising:

forming a source region and a drain region in a substrate that are separated by a channel region in the substrate;

forming an insulating layer on the substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0; and

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the substrate.

44. The method of claim 43 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

45. The method of claim 43, further comprising:

forming a well region in the substrate;

forming field oxide on the substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching.

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46. (Amended) The method of claim 43 wherein:

forming a source region comprises forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate; and

further comprising:

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

47. (Amended) The method of claim 43 wherein:

forming a source region comprises forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate; and

further comprising:

oxidizing the gate by plasma oxidation to form an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

48. The method of claim 43, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant.

49. The method of claim 43, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation.

50. (Twice Amended) A method of fabricating a transistor comprising:

forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

forming an insulating layer on the silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation; and

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the silicon substrate.

51. The method of claim 50 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

52. The method of claim 50, further comprising:

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

doping the layer comprises doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer

to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching.

53. (Amended) The method of claim 50, further comprising:

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

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depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

54. (Amended) The method of claim 50, further comprising:

oxidizing the gate by plasma oxidation to form an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

55. (Twice Amended) A method of fabricating a transistor comprising:

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forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

forming an insulating layer on the silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation; and

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a gate on the silicon substrate.

56. The method of claim 55 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low

temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

57. The method of claim 55, further comprising:

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of gate oxide or a layer of tunnel oxide on a silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching.

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58. (Amended) The method of claim 55, further comprising:

oxidizing the gate by plasma oxidation to form a layer of oxide on the gate; and

depositing oxide over the gate, the source region, and the drain region by chemical vapor deposition.

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59. (Amended) The method of claim 55, further comprising:

oxidizing the gate by plasma oxidation to form an intergate dielectric on the gate; and

forming a polysilicon control gate over the intergate dielectric.

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60. (Twice Amended) A method of fabricating a floating gate transistor comprising:

forming a source region and a drain region in a substrate that are separated by a channel region in the substrate;

forming an insulating layer on the substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric.

61. The method of claim 60 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

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62. (Twice Amended) The method of claim 60, further comprising:

forming a well region in the substrate;

forming field oxide on the substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide

compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming a source region comprises forming a source region and a drain region in a silicon substrate that are separated by a channel region in the substrate;

wherein forming an insulating layer comprises forming a layer of tunnel oxide on the silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric.

63. The method of claim 60, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant.

64. The method of claim 60, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation.

65. (Twice Amended) A method of fabricating a floating gate transistor comprising:

forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

forming an insulating layer on the silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the silicon substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric.

66. The method of claim 65 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

67. (Twice Amended) The method of claim 65, further comprising:

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of tunnel oxide on the silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the

insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric.

68. (Twice Amended) A method of fabricating a memory cell comprising:

forming a source region and a drain region in a substrate that are separated by a channel region in the substrate;

forming an insulating layer on the substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric that is coupled to receive a control voltage from a memory device.

69. The method of claim 68 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low

temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

70. (Twice Amended) The method of claim 68, further comprising:

forming a well region in the substrate;

forming field oxide on the substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming a source region comprises forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

wherein forming an insulating layer comprises forming a layer of tunnel oxide on the silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric that is coupled to receive a programming voltage or a read voltage from a memory device.

71. The method of claim 68, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with a p-type implantation of a boron dopant.

72. The method of claim 68, further comprising doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation.

73. (Twice Amended)A method of fabricating a memory cell comprising:

forming a source region and a drain region in a silicon substrate that are separated by a channel region in the silicon substrate;

forming an insulating layer on the silicon substrate;

forming a layer of a silicon carbide compound $Si_{1-x}C_x$ on the insulating layer wherein x is between 0 and 1.0;

doping the layer of the silicon carbide compound $Si_{1-x}C_x$ with an n-type ion implantation;

D12 removing portions of the insulating layer and the layer of the silicon carbide compound $Si_{1-x}C_x$ to form a floating gate on the silicon substrate;

forming an intergate dielectric on the floating gate; and

forming a control gate over the intergate dielectric that is coupled to receive a control voltage from a memory device.

74. The method of claim 73 wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ further comprises depositing the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer by low pressure chemical vapor deposition, or by low pressure rapid thermal chemical vapor deposition, or by decomposition of hexamethyl disalene using ArF excimer laser irradiation, or by low temperature molecular beam epitaxy, or by reactive magnetron sputtering, or by DC plasma discharge, or by ion-beam assisted deposition, or by ion-beam synthesis, or by laser crystallization, or by laser reactive ablation deposition, or by epitaxial growth by vacuum anneal.

75. (Twice Amended) The method of claim 73, further comprising:

forming a well region in the silicon substrate;

forming field oxide on the silicon substrate to define an active region;

doping the silicon carbide compound $Si_{1-x}C_x$ while forming the layer of the silicon carbide compound $Si_{1-x}C_x$ on the insulating layer; and

wherein forming an insulating layer comprises forming a layer of tunnel oxide on the silicon substrate by dry thermal oxidation;

wherein forming a layer of a silicon carbide compound $Si_{1-x}C_x$ comprises depositing a film of a polycrystalline or microcrystalline doped silicon carbide compound $Si_{1-x}C_x$ on the insulating layer;

wherein removing comprises:

patterning the layer of the silicon carbide compound $Si_{1-x}C_x$; and

etching the layer of the silicon carbide compound $Si_{1-x}C_x$ and the insulating layer to form a floating gate with plasma etching, or reactive ion etching, or a combination of plasma etching and reactive ion etching;

wherein forming an intergate dielectric comprises oxidizing the floating gate by plasma oxidation to form an intergate dielectric on the floating gate; and

wherein forming a control gate comprises forming a polysilicon control gate over the intergate dielectric that is coupled to receive a programming voltage or a read voltage from a memory device.